

REMARKS

Claims 1-24 are pending in the present application. Claims 1, 5, 8, 9, 13, 16, 17, 21, 23 and 24 are amended. Claims 1, 9, and 17 are amended to recite "routing nets between a source and one or more associated sinks; and selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink." These features are supported at least on page 10, lines 29-32, and on page 22, line 4 to page 25, line 4.

Claims 5, 13, and 21 are amended to recite "wherein the selectively assigning step includes computing a cost, $q(v)$, for using a buffer in a particular tile and the cost, $q(v)$, is given by the equation:

$$q(v) = \begin{cases} \frac{p(v)(b(v)+1)}{B(v)-b(v)} & \text{if } \frac{b(v)}{B(v)} < 1 \\ \infty & \text{otherwise} \end{cases}$$

wherein $p(v)$ is a sum of probabilities for tile v over all unprocessed nets, wherein $b(v)$ is a current number of used buffer sites, and wherein $B(v)$ is a number of buffer sites in tile v . These features are supported at least on page 20, lines 23-27 of the current specification. Claims 8, 16, and 24 are amended to be consistent with independent claims 1, 9, and 17. Claim 23 is amended to provide proper antecedent basis and correct a minor error. Reconsideration of the above amendment of claims in view of the following Remarks is respectfully requested.

I. Obviousness-type Double Patenting

The Examiner has rejected claims 1, 9, 17 in combination with dependent claims 2, 10, and 18 under the judicially-created doctrine of obviousness-type double patenting as being unpatentable in view of claims 1, 8, and 15 of U.S. Patent No. 6,401,234.

Applicants have submitted herewith a terminal disclaimer under 37 CFR § 1.321, thus obviating the double patenting rejection. Applicants respectfully request that the rejection be withdrawn.

In addition, the Examiner has rejected claims 1, 9, 17 in combination with dependent claims 2, 10, and 18 under the judicially-created doctrine of obviousness-type double patenting as being unpatentable in view of claims 1, 20, 39, and 45 of U.S. Patent No. 6,591,411. Applicants have submitted herewith a terminal disclaimer under 37 CFR § 1.321, thus obviating the double patenting rejection. Applicants respectfully request that the rejection be withdrawn.

II. 35 U.S.C. § 112, Second Paragraph, claims 5, 13, and 21

The Examiner has rejected claims 5, 13, and 21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

The Office Action stated that although the submission of Figure 7 and the description in Applicant's specification provide enabling support for the formula in dependent claims 5, 13, and 21, within the claims themselves, there is no disclosure as to what the "meets and bounds" are for the disclosed terms, " $b(v)$, $p(v)$, and $B(v)$ ".

By this Response, claims 5, 13, and 21 are amended to recite "wherein the selectively assigning step includes computing a cost, $q(v)$, for using a buffer in a particular tile and the cost, $q(v)$, is given by the equation:

$$q(v) = \begin{cases} \frac{p(v)+b(v)+1}{B(v)-b(v)} \cdot \frac{b(v)}{p(v)} < 1 \\ \infty & \text{otherwise} \end{cases}$$

wherein $p(v)$ is a sum of probabilities for tile v over all unprocessed nets, wherein $b(v)$ is a current number of used buffer sites, and wherein $B(v)$ is a number of buffer sites in tile v . Therefore, the terms " $b(v)$, $p(v)$, and $B(v)$ " are now defined in claims 5, 13, and 21. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 5, 13, and 21 under 35 U.S.C. § 112, second paragraph.

III. Allowable Subject Matter, claims 5-8, 13-16, and 21-24

Applicants thank Examiner Craig for the indication of allowable subject matter in claims 5-8, 13-16, and 21-24. However, for the reasons set forth hereafter, Applicants respectfully submit that all of the claims are directed to allowable subject matter and that the application is in condition for allowance.

IV. 35 U.S.C. § 102(b), Alleged Anticipation, claims 1, 2, 9, 10, 17 and 18

The Office Action rejects claims 1, 2, 9, 10, 17, and 18 under 35 U.S.C. § 102(b) as being allegedly anticipated by Varadarajan et al. (U.S. 5,838,583). This rejection is respectfully traversed.

With regard to claims 1, 9, and 17, the Office Action states:

As to claims 1, 9, and 17, the Office Action states:

As regards independent claims 1, 9, and 17 the *Varadarajan et al.* reference teaches, routing (Figures 19a, 19b and 19c, Col. 2 Lines 28-43), tiles (Figure 2, Items 311, 313, Col. 25 Lines 27-58), cost calculations (Figure 16b item 253, Col. 23 Lines 4-37).

Office Action dated December 14, 2004, page 5.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 21 U.S.P.Q.2d 1031, 1034 (Fed Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). Applicants respectfully submit that Varadarajan does not teach every element of the claimed invention arranged as they are in claims 1, 9, and 17. Specifically, Varadarajan does not teach routing nets between a source and one or more associated sinks or selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm

for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink.

Amended independent claim 1, which is representative of claims 9 and 17, recites:

1. A method for designing buffer and wire placement in an integrated circuit, the method comprising:
 - representing the surface of a integrated circuit design as a tile graph;
 - receiving an allocation of buffer locations for selected tiles in the tile graph;
 - routing nets between a source and one or more associated sinks; and
 - selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink.

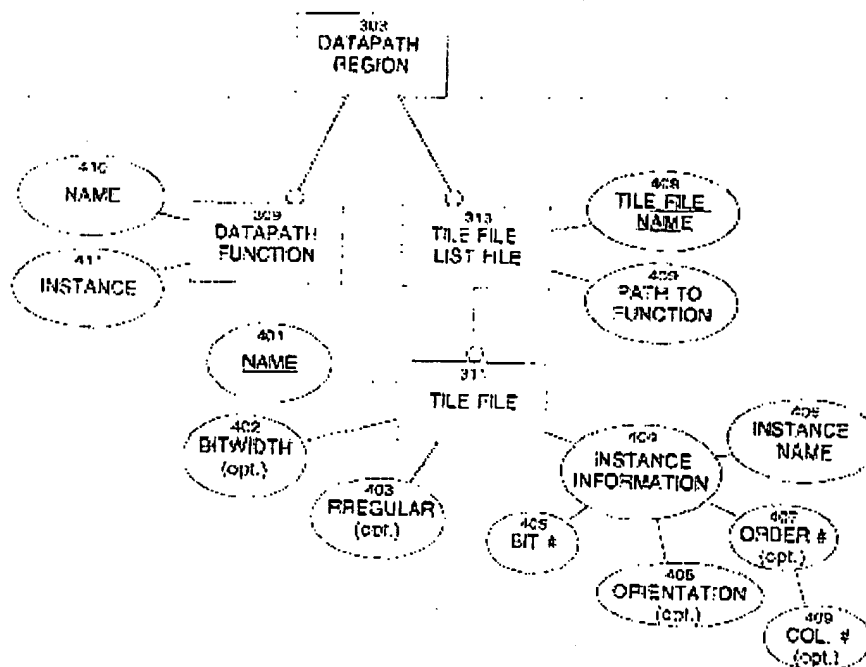
Varadarajan does not teach the features emphasized above. As discussed in the Abstract, Varadarajan teaches a system that includes a datapath floorplanner, a datapath placer, and routing space estimator. The datapath floorplanner allows designers to establish planning operations datapath regions that include a number of datapath functions each. The datapath floorplanner creates datapath regions from a netlist specifying logic cell instances and connectivity information, and from a plurality of tile files. The datapath placer places datapath functions in each region using relative placement information and constraints. The routing space estimator estimates the space needed for routing a placed region.

However, Varadarajan does not teach routing nets between a source and one or more associated sinks. The Office Action alleges that Varadarajan teaches these features at column 2, lines 28-43, and column 25, lines 27-58. In the first section, Varadarajan teaches a system and method that defines datapath regions including datapath functions in the circuit and provides this information to a placement system for determining the placement of logic cells in the datapath functions, while preserving the regularity of the datapath. In the second section, Varadarajan teaches a tiler that produces a detailed placement of all logic cell instances within each of the datapath functions in the linear order. The tiler traverses all the datapath functions in the datapath region in the given linear order and using instance information (bit#, column#, and order#) in the tile file

along with the appropriate inter-function or inter-bit spacing numbers, as determined by the routing space estimator to determine the actual placement of the logic cell instance.

However, none of the above sections mention anything about routing nets between a source and one or more associated sinks. In fact, Varadarajan does not even mention anything about a source or one or more associated sinks. At column 6, lines 30-58, Varadarajan merely teaches that the datapath placer automatically determines the bit offset of each datapath function in its datapath region with respect to the databus associated with the function, wherein the datapath functions are vertically aligned with databuses running horizontally through the datapath functions. Thus, Varadarajan is only concerned with determining a bit offset of the datapath function relative to the range of bits in the databus. Varadarajan does not teach or suggest anything about a source or one or more associated sinks, let alone routing nets between a source and one or more associated sinks. Therefore, Varadarajan does not teach routing nets between a source and one or more associated sinks.

In addition, Varadarajan does not teach selectively assigning buffer locations within selected tiles based upon buffer needs of the nets. To the contrary, placements of logic cells are determined based on the instance information in the tile file, not buffer needs of the nets. As described in the second section above and in Figure 4 as shown below, Varadarajan merely teaches that tile files 311 capture relative placement of instances with single datapath function 309, and specifies for each instance in a single datapath function instance information 404 that specifies a name of the instance, the relative horizontal (column # 409 and order # 407) and vertical position (bit # 405) of the instance and its orientation 408 (column 8, lines 4-12). Therefore, Varadarajan does not teach assigning buffer locations within selected tiles based upon buffer needs of the nets.



Furthermore, Varadarajan does not teach that the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink. The Office Action alleges that Varadarajan teaches a cost minimization algorithm at column 23, lines 4-37, where Varadarajan teaches cost functions for the datapath placer. At column 18, line 47 to column 19, line 10, Varadarajan teaches that a specific ordering of nodes in a state space graph is determined by optimizing a cost function on each of the nodes. The cost of each node is determined using an estimated wire length cost function, an estimated overflow track cost function, and an estimated wasted area cost function. Thus, the cost functions of Varadarajan are different from the cost minimization algorithm in that the cost functions do not determine a cost array for buffer placement. Rather, the cost functions are used to estimate wire length cost, overflow track cost, and wasted area cost.

Even if the cost functions determine a cost array for buffer placement, the cost functions of Varadarajan still do not compute the cost array using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink. As discussed above, Varadarajan is only concerned with determining a bit offset of the datapath function relative to the range of bits in the databus. Varadarajan is not concerned with routing nets between a source and one or more associated sinks. Therefore, Varadarajan does not and would not teach a cost minimization algorithm that computes a cost array for buffer placement using a single-sink buffer insertion algorithm for one associated sink and a multi-sink buffer insertion algorithm for more than one associated sink. Therefore, Varadarajan fails to teach the features of claims 1, 9, and 17 of the present invention.

In view of the above, Applicants respectfully submit that Varadarajan does not teach each and every feature of claims 1, 9, and 17. At least by virtue of their dependency on claims 1, 9 and 17 respectively, Varadarajan does not teach the features of dependent claims 2, 10, and 18. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1, 2, 9, 10, 17, and 18 under 35 U.S.C. § 102(b).

V. **35 U.S.C. § 102(e), Alleged Anticipation, claims 1-4, 9-12, and 17-20**

The Office Action rejects claims 1-4, 9-12, and 17-20 under 35 U.S.C. § 102(e) as being allegedly anticipated by Nitta et al. (Pub. No. U.S. 2001/009031). This rejection is respectfully traversed.

With regard to claims 1, 9, and 17, the Office Action states:

As regards independent claims 1, 9, and 17, the *Nitta et al.* reference teaches, a method for designing buffer and wire placement in an integrated circuit (Figure 5, paragraphs 0002 & 0003), representing the surface of a integrated circuit as a tile graph (Figures 1-4 and paragraphs 0015, 0016, 0017, 0018, 0019, 0020, and 0021 which teach "blocks" which are functionally equivalent to "tiles"), receiving an allocation of buffer locations for selected files in the tile graph (The Examiner notes that it would be inherent that buffers would be placed on an integrated circuit and that the reference discloses routing of "cells" Figure 5 Item 16), routing nets between associated sources and sinks "a prohibiting region" is functionally equivalent to a "sink" (Figures 12A, 12B, 12C), selectively assigning buffer locations within selected tiles

(Figures 17B, 17A paragraph 0069), assign(ing) buffer locations using a cost minimization algorithm (Figures 15A & 15B).

Office Action dated December 14, 2004, page 6.

Nitta does not teach routing nets between a source and one or more associated sinks or selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink.

Similar to Varadarajan, Nitta also does not teach routing nets between a source and one or more associated sinks. As discussed in the Abstract, Nitta teaches a global routing method that first generates a Steiner tree without any layers, prohibition, or wiring capacity constraints. In consideration of the prohibition region, wiring capacity, and layers, partial correction of Steiner tree is repeated so as not to increase a line length as far as possible. The Steiner tree is corrected generating a path collection obtained by dividing the Steiner tree into a plurality of paths each having at least a Steiner point, as a value, being an intersection of 3 or more branches.

The Office Action alleges that Nitta teaches the features of claims 1, 9, and 17 of the present invention in Figures 12A, 12B, and 12C, and states that a prohibiting region is functionally equivalent to a "sink." Applicants respectfully disagree. Figures 12A, 12B, and 12C of Nitta are shown below:

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FIG. 12A

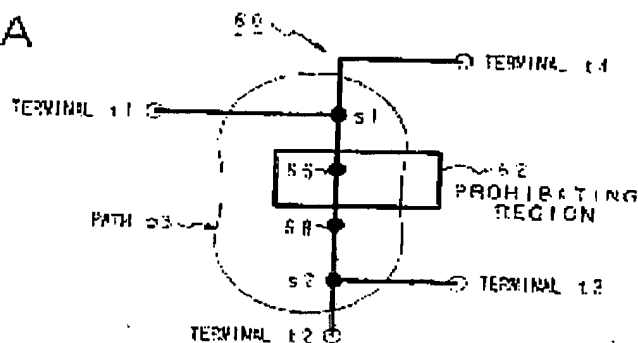


FIG. 12B

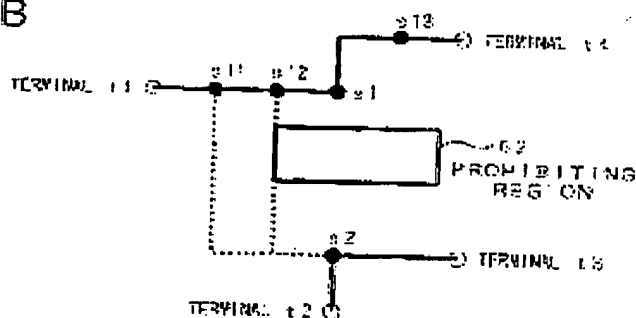
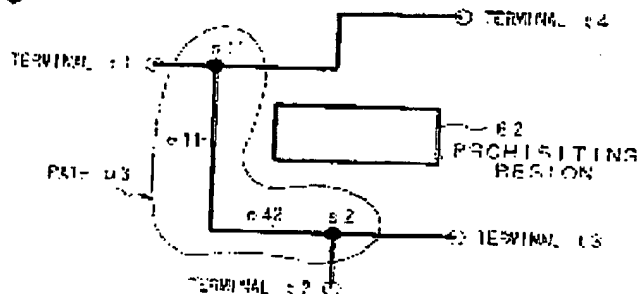


FIG. 12C



As shown in **Figures 12A, 12B, and 12C** and described in paragraph 0064, Nitta teaches correcting a path that passes through the wiring prohibition region to a path that routes around the wiring prohibition region. Thus, the prohibition region is merely an area in a grid that prohibits passing wires or nets. The prohibition region is not functionally equivalent to a "sink" as alleged by the Examiner. On page 10, lines 27-30 of the current specification, a net is simply a set of cells or pins to be connected together and these pins can be classified as either drivers or sinks. Each net has one driver and

one or more sinks. Thus, a sink is a pin connected to a net. This is different from a prohibition region, which prohibits passing of a net. Therefore, Nitta does not teach routing nets between a source and one or more associated sinks, as recited in claims 1, 9, and 17.

In addition, Nitta does not teach that the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink. The Office Action alleges that Nitta teaches the above features in **Figures 15A, 15B**, wherein Nitta teaches a length improvement process of the Steiner tree. However, the process as illustrated in **Figures 15A and 15B** is based on the shortest Manhattan distance from the start and end point of a path, which is a distance of a straight line connected between two points (paragraph 0067). The length improvement process is not based on a cost minimization algorithm. Therefore, Nitta fails to teach a cost minimization algorithm, and would not teach a cost array for buffer placement that is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink.

Furthermore, the Office Action alleges that Nitta teaches selectively assigning buffer locations within selected tiles based upon buffer needs of the nets in **Figures 17A and 17B**, as shown below and in paragraph 0069. However, in **Figures 17A, 17B**, and paragraph 0069, Nitta merely teaches examples of allotment processing of branches to layers performed after partial correction for and line improvement on a Steiner tree. The Steiner tree 60 is first allotted to the first layer and then to the second layer based on layer information inputted in advance. A solution of global routing for wiring trees T1 to Tn of nets N1 to Nn is outputted to the output unit.

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FIG. 17A

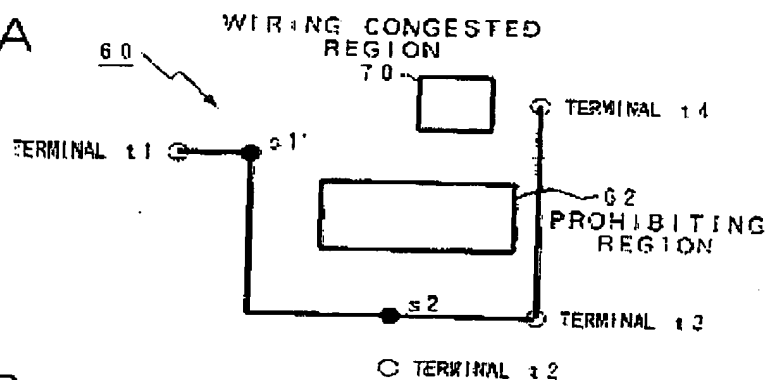
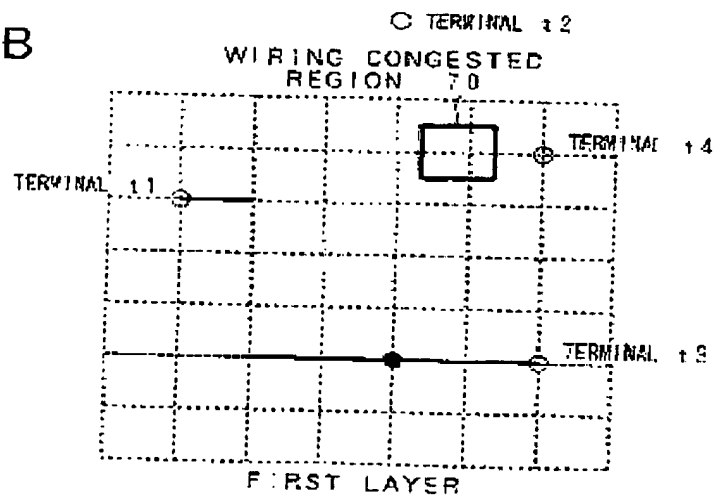


FIG. 17B



Thus, Nitta merely teaches how to allot Steiner tree branches to two different layers in order to avoid wiring congested region. Nitta does not teach how to assign buffer locations within selected tiles, let alone assigning buffer locations within selected tiles based upon buffer needs of the nets, as recited in claims 1, 9, and 17.

In view of the above, Applicants respectfully submit that Nitta does not teach each and every feature of claims 1, 9, and 17. At least by virtue of their dependency on claims 1, 9 and 17 respectively, Nitta does not teach the features of dependent claims 2-4, 10-12, and 18-20. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1-4, 9-12, and 17-20 under 35 U.S.C. § 102(c).

VI. **35 U.S.C. § 102(e), Alleged Anticipation, claims 1, 2, 9, 10, 17, and 18**

The Office Action rejects claims 1, 2, 9, 10, 17, and 18 under 35 U.S.C. § 102(e) as being allegedly anticipated by Koh et al. (Manhattan or Non-Manhattan? A Study of Alternative VLSI Routing Architectures, ACM 2000, pages 47-52). This rejection is respectfully traversed.

With regard to claims 1, 9, and 17, the Office Action states:

As regards independent claims 1, 9, and 17 the Koh et al. reference teaches, routing (page 47 & page 48), tiles (page 48), cost calculations (page 51).

Office Action dated December 14, 2004, page 7.

Just like Varadarajan and Nitta above, Koh does not teach selectively assigning buffer locations within selected tiles based upon buffer needs of the nets, wherein the nets are routed through selected tiles and assigned buffer locations using a cost minimization algorithm, and wherein a cost array of the cost minimization algorithm for buffer placement is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one associated sink. As discussed in the Abstract, Koh teaches a non-Manhattan Steiner tree heuristic that reduces wire lengths by 17% and a graph-based interconnect optimization algorithm that allows performance optimization beyond what can be obtained through wire length reduction alone.

The Office Action alleges that Koh teaches the features of independent claims 1, 9, and 17 on pages 47, 48, and 51. However, on page 48, Koh merely teaches employing a non-Manhattan Steiner tree algorithm that is derived from an edge-removal algorithm. The new algorithm repeatedly joints a vertex to an existing edge and then removes an edge on a generated cycle. The "merge" function which joins the vertex to the edge has been modified for the new routing metrics. Thus, Koh's algorithm is based on the removal of tile edges. Koh's algorithm has nothing to do with a cost array for buffer placement, let alone a cost array that is computed using a single-sink buffer insertion algorithm for one associated sink and a multi-sink buffer insertion algorithm for more than one associated sink.

On page 51, Koh teaches that the benefits of wire length reduction may outweigh the additional via cost. Vias are required, according to table 3 on page 52, to connect the pins to the interconnect nets. However, Koh still fail to mention selectively assigning buffer locations within selected tiles based upon buffer needs of the net or routing the net through selected tiles and assigned buffer locations based on a cost minimization algorithm. Therefore, Koh does not teach the features of claims 1, 9, and 17 of the present invention.

In view of the above, Applicants respectfully submit that Koh does not teach each and every feature of claims 1, 9, and 17. At least by virtue of their dependency on claims 1, 9 and 17 respectively, Koh does not teach the features of dependent claims 2, 10, and 18. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1, 2, 9, 10, 17 and 18 under 35 U.S.C. § 102(e).

VII. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 3/14/05

Respectfully submitted,



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